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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/842,333	04/25/2001	Brian William Hughes	10004547-1	7542

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EXAMINER	
ABRAHAM, ESAW T	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 12/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/842,333	HUGHES ET AL.	
	Examiner	Art Unit	
	Esaw T Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8-11,15-17 and 19* is/are rejected.

7)☒ Claim(s) *7,12,14 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims **1 to 19** are presented for examination.

Claim objections

2. Claims **7, 14, 15 and 19** are objected to because of the following informalities:

(a) Please change the term "an memory" to "a memory" (in claim 15 line 1)

(b) Please add "to" after or next to the term "equal" (see claims 7, 14 and 19).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims **1 to 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Toshiaki et al. (U.S. PN: 5,555,212) Fujimoto (U.S. PN: 6,145,05).

As per claims **1 and 9,** Toshiaki et al. teach a method and apparatus for redundancy word line replacement (repairing) in a semiconductor device involves generating a control signal which causes the data on the data lines to be flipped when the bit pattern of the memory cells coupled to a redundant word line are complementary to the bit pattern of the memory cells of a defective word line which is being replaced by the redundant word line (see col. 1, lines 7-11). Further, Toshiaki et al. teach a method for testing a semiconductor memory device including normal memory cells and redundant memory cells wherein the normal memory cells are connected to normal word lines and the redundant memory cells are connected to redundant word lines and further the method comprising the steps of detecting (error locating) a defective memory cell in a normal memory cell array, inhibiting a normal word line connected to said detected defective memory cell from being accessed, and replacing the defective memory cell with a redundant memory cell connected to a redundant word line (see claim 1 and claim 30). Furthermore, Toshiaki et al. teach a semiconductor device memory cells arranged in rows and columns, the memory cells including normal memory cells and redundant memory cells for replacing defective ones of the normal memory cells and further a data flip circuit selectively flips data signals on first and second I/O lines (see col. 4, lines 3-19).Toshiaki et al. **do not explicitly** teach inhibiting subsequent repairing of number of elements (memory cells). **However,** Fujimoto in an analogous art teaches a cache memory having flags for inhibiting rewrite of replacement algorithm corresponding to fault cell (see the title). Fujimoto further teaches cache memory which employs plural-way set associative system and replaces data of a way specified by an algorithm for updating data based on previous reference record, comprising

reference history storage areas which are provided for each entry updated and indicate the previous reference record, and are referred to at the time of replacement so as to indicate a way in which the data is to be replaced; and rewrite inhibit flags which are provided corresponding to said reference history storage areas to inhibit rewrite of said reference history storage areas, wherein when a fault entry is found in the initial state at the time of power-on (see claim 1). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to implement the teachings of Toshiaki to employ a process for setting an inhibit flag for performing an inhibiting operation as taught by Fujimoto. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated in order to avoid the fault cells regardless of the quantity of the fault cells with a simple and small structure and easy control and further increase the data reading speed (see col. 7, lines 10-17).

As per claims **2 and 10,** Toshiaki et al. in view of Fujimoto teach all the subject matter claimed in claims 1 and 9 including Fujimoto teach a processing system (21) as shown in FIG. 2. Updating of the LRU bit 4 and set/reset of the LRU rewrite inhibit flag 10 are carried out according to an instruction from the processor 17 of the system 21 based on a result of detection of the fault cell (see col. 6, lines 20-28).

As per claims **3 and 11,** Toshiaki et al. in view of Fujimoto teach all the subject matter claimed in claims 1 and 9 including Toshiaki et al. teach a method and apparatus for replacing defective memory cells in a semiconductor memory device using redundant memory cells (see col. 1, lines 8-11). Fujimoto further teaches a cache memory which employs plural-way set associative system and replaces data of a way specified by an algorithm for updating data based

on previous reference record, comprising: reference history storage areas which are provided for each entry commonly to each way and updated according to the algorithm, indicate the previous reference record, and are referred to at the time of replace so as to indicate a way in which the data is to be replaced; and rewrite inhibit flags which are provided corresponding to the reference history storage areas to inhibit rewrite of the reference history storage areas (see col. 3, lines 1-18).

As per claim **4,** Toshiaki et al. in view of Fujimoto teach all the subject matter claimed in claim 1 including Toshiaki et al. teach a semiconductor device includes memory cells arranged in rows and columns, the memory cells including normal memory cells and redundant memory cells for replacing defective ones of the normal memory cells (see col. 4, lines 3-19).

As per claim **5,** Toshiaki et al. in view of Fujimoto teach all the subject matter claimed in claims 1 and 4 including Toshiaki et al. teach a semiconductor device includes memory cells arranged in rows and columns, the memory cells including normal memory cells and redundant memory cells for replacing defective ones of the normal memory cells (see col. 4, lines 3-19). Toshiaki et al. **do not teach** initializing a row register or a column register is before or prior to the step of testing. **However,** the practice of initialization before testing is known in the art since row registers or column registers must first initialized (setting addresses or contents of storage to zero or other starting values at the beginning of, or at the prescribed points in) and by virtue of the fact row/column registers must be initialized or configured before testing any storage sub elements in a the memory system. **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to initialize registers before testing. **This modification** would have been obvious because a person having

ordinary skill in the art would have been motivated to do so because initializing or configuring registers before testing are well known futures of memory testing systems.

As per claims **8 and 13,** Toshiaki et al. in view of Fujimoto teach all the subject matter claimed in claims 1, 9. Toshiaki et al. in view of Fujimoto **do not teach** incrementing column and row register. **However,** the step of incrementing row or column registers is known in the computer art because in a computer, a register is one of a small set of data holding places that are part of a computer processor wherein the data are commonly incremented or decremented for further computations. **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to increment row and column registers. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because the steps of incrementing row or column registers are well known futures of computer processors.

4. Claims 15-**19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Maeda (U.S. PN: 5,568,408) in view of Fujimoto (U.S. PN: 6,145,05).

As per claim **15-17,** Maeda teach an automatic repair data editing system is associated with a repairing system for rescuing defective semiconductor memories fabricated on semiconductor wafers from rejection further the system edits repair data that is partially duplicated due to a trouble in the repairing system, and allows the repairing system to automatically carry out a repair work on the defective semiconductor memories (abstract). Further, the automatic repair data editing system comprising a repair data producing means (repair logic) for performing test sequence for each semiconductor integrated circuit fabricated on semiconductor wafers and for producing pieces of repair data used for rescuing defective

semiconductor integrated circuits, an editing means (compare circuitry) for comparing pieces of second identity data with pieces of first identity data to determine if the pieces of repair data contain duplicate pieces of repair data and the editing means further deleting the duplicate pieces from said pieces of repair data (claim 1). Maeda **does not explicitly teach** an inhibit circuitry for that prevents the repair logic from operating on the memory elements. **However,** Fujimoto in an analogous art teaches a cache memory having flags for inhibiting rewrite of replacement algorithm corresponding to fault cell (see the title). Fujimoto further teaches cache memory which employs plural-way set associative system and replaces data of a way specified by an algorithm for updating data based on previous reference record, comprising reference history storage areas which are provided for each entry updated and indicate the previous reference record, and are referred to at the time of replacement so as to indicate a way in which the data is to be replaced; and rewrite inhibit flags which are provided corresponding to said reference history storage areas to inhibit rewrite of said reference history storage areas, wherein when a fault entry is found in the initial state at the time of power-on (see claim 1). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to implement the teachings of Toshiaki to employ a process for setting an inhibit flag for performing an inhibiting operation as taught by Fujimoto. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated in order to avoid the fault cells regardless of the quantity of the fault cells with a simple and small structure and easy control and further increase the data reading speed (see col. 7, lines 10-17).

Allowable subject matter

5. Claims **6, 7, 12, 14, and 18** are objected to as being dependent upon a rejected base claim but would be allowable if rewritten independent from including all of the limitation of the base claim and any intervening claims. The claimed invention comprises the step of means for inhibiting comprises means for checking, after detecting an error, whether an inhibit flag which prevents the step or repairing from subsequently operating on elements of the group on N elements is set; and if the inhibit flag has not been set, sending a row address of the element to rows repair logic for performing the step of repairing the step of repairing and setting the inhibit flag; and if the inhibit flag has been set, inhibit operation of the row repair logic (**as in claims 6, 12 and 15**) which the prior art do not teach or render obvious.

Claims **7 and 14,** which are directly or indirectly dependents of claims 6 and 12 are also objected.

Claim **18,** which is directly or indirectly dependents of claim 15 is also objected.

Conclusion

6. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3812. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Esaw Abraham

Esaw Abraham

Art unit: 2133